600W DC/DC Converter for Server SMPS: design guidelines

IFAT PMM Application and Systems
Francesco Di Domenico
Olivier Guillemant
Datacenter Servers and SMPS

Server SMPS typical spec. requirements

HV DC/DC Converter Design Guidelines: LLC topology

Synchronous Rectification optimization in LLC
Data Centers are today part of our daily life
SMPS in the Datacenters

Data Center

Server

SMPS
Server form factors

Rack mounted
- Height: 1U/2U/4U
- 1/2/4 processors per board
- 75 W-150W processors
- PSU
  - Up to 3: 600W, 750W & 1,2kW.

Blade mounted
- Height: ½U/1U
- 1/2 processors per board
- 75W – 95W processors
- PSU
  - Up to 4: 950W ~ 1,5kW
  - 1,2kW for High Line.
  - 800W~900W for low line.
  - Up to 6: 960W ~ 2,7kW

Work station
- Desktop PC like form factor
- 1/2/4 processors per board
- 40W-150W processors
- PSU
  - 550W / 430W x 2
  - 600W ~ 920W.

Mainframe Server
- Multi-rack Server
- Multiple processors within Server unit
- 95W-150W processors
- Power consumption ranges from 4,5kW ~ 10kW.
How do big OEMs react?

High End Platforms

- Reliability

Efficiency

Low Risk

Low End Platforms

- Cost

Commonality
Key-words in Server arena

- Field PPM targets expect to decrease 15% YTY
- Technical choices mainly made due to cost, not performance
- Leveraging solutions across different products and brands: compact form factor helps
- Reduces development and qualification expense
- Time-to-market shrinking, reducing regression testing.
- Development expanding to low cost Geographies.
- Custom or off-the-shelf assemblies selected for potential use in as many releases as possible (compact form factor helps)
Typical steps in a new Project (in particular in the design of Power Architecture)
Specific activities at supplier site (coordinated by OEM Development)

<table>
<thead>
<tr>
<th>Phase</th>
<th>Supplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product Definition</td>
<td>Supplier presents latest to OEM technologies for evaluation and possible integration into new projects.</td>
</tr>
<tr>
<td>Concept Design</td>
<td>OEM communicates system level requirements, supplier provides comprehensive card level solutions.</td>
</tr>
<tr>
<td>RFQ Prep/Review</td>
<td>Performs electrical and thermal simulations. Engineering specification section-by-section confirmation of ability to meet requirements.</td>
</tr>
<tr>
<td>Detailed Design</td>
<td>Provide ongoing feedback to design requirements, risk assessments, and suggestions to enhance design robustness. Coordinate design reviews with OEM development, qualification, 1st and 2nd tier suppliers.</td>
</tr>
<tr>
<td>Unit Level Test</td>
<td>Evaluate critical component waveforms as well as inputs/outputs according to specification.</td>
</tr>
<tr>
<td>System Test</td>
<td>Provide complete end to end long term risk assessment for both performance and procurement issues: component de-rating guidelines, “disaster recovery” plans, cost reduction opportunities due to commonality.</td>
</tr>
<tr>
<td>Production/Quality Mgmt</td>
<td>Provide ongoing feedback of line data and early warning on trends. Coordinate 1st and 2nd tier response to line and field problems.</td>
</tr>
</tbody>
</table>
Main responsibilities at OEM’s Power Development site

- Power Subsystem Architecture definition.
- Selection of Commercial Off-the-Shelf power conversion components.
- Translating system requirements into Engineering Specifications.
- Unit level testing/functional verification.
- System integration, e.g. verification of redundant operation.
- Review of vendor and final unit level qualification.
- Provide support for line and field issues post GA
An emerging issue for datacenters: the energy bill. How to reduce it?

- High voltage distribution
- Use of DC power
- Highly efficient UPS systems
- Efficient redundancy strategies

- Load management
- Virtualization
- Server innovation
- Heat recovery

- Better air management
- Better environmental conditions
- Move to liquid cooling

- Rejected heat for cooling
- Use of renewable energy/fuel cells
- Eliminate transmission losses

Reduction of source and transmission losses
Present and potential future scenarios

**Today:**

\[ \Delta / Y \]

**Scenario 1:**
still AC/DC input BUT centralized PFC within rack

**Scenario 2:**
all over DC/DC power distribution

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HV DC Bus Worldwide Data Center

Cloud Computing and Virtualization

- **Cloud Computing:**
  Software/Storage/Computing power is delivered by “the Cloud” to client devices (Smartphones, Tablets, Laptops ...). The “cloud” is a Server/Computing infrastructure. The rapid growth of client devices will drive the growth of servers for cloud computing.

- **Virtualization:**
  Virtualization refers to the simulation of hardware through software. Eg: instead of employing 3 physical servers for e-mail/web/storage only one physical but virtualized server can take over the same tasks. This trend increases server utilization but reduces the amount of required new server installments.
Impact of the need of energy bill reduction/new trends on the PSU units

Future trend...
EFFICIENCY & POWER DENSITY

5 years ago
10W / inch³

Now
30W / inch³

5 years in the future

<table>
<thead>
<tr>
<th>Load</th>
<th>10%</th>
<th>20%</th>
<th>50%</th>
<th>100%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>90%</td>
<td>94%</td>
<td>96%</td>
<td>91%</td>
</tr>
</tbody>
</table>

Load

<table>
<thead>
<tr>
<th>Efficiency</th>
<th>10%</th>
<th>20%</th>
<th>50%</th>
<th>100%</th>
</tr>
</thead>
<tbody>
<tr>
<td>10%</td>
<td>80%</td>
<td>81%</td>
<td>81%</td>
<td>81%</td>
</tr>
<tr>
<td>20%</td>
<td>82%</td>
<td>85%</td>
<td>85%</td>
<td>85%</td>
</tr>
<tr>
<td>50%</td>
<td>85%</td>
<td>88%</td>
<td>88%</td>
<td>87%</td>
</tr>
<tr>
<td>100%</td>
<td>85%</td>
<td>90%</td>
<td>92%</td>
<td>88%</td>
</tr>
</tbody>
</table>

10W / inch³

30W / inch³

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Impact of PSU efficiency in annual savings (source: Lawrence Berkeley National Lab. - 2010)

Annual cost saving per server using Platinum vs. Standard 80+ SMPS
Impact of PSU efficiency in annual savings (source: Lawrence Berkeley National Lab.- 2010)
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Example
SMPS for servers

CoolMOS™

HV DC/DC
• I-TTF
• LLC
• ZVS FB PS

CoolSET™

Aux SMPS
• DCM Flyback
• QR Flyback

Sync + ORing Rect.

OptiMOS™

PFC
• Classic
• Interleaved
• Bridgeless

SiC Diode™

TDA486x™

Analog Controller

ICExPCS0x™

ICExHS01G™

85 ~ 265VAC

Converter’s XFMR

IC Driver

Gate XFMR

Optocoupler

Secondary Digital Controller

IC Driver

Gate XFMR

UART or PMBus

5V/12V

12V

Analog Controller
Full Digital Solution

- **PFC**
  - Classic

- **HV DC/DC**
  - LLC

- **Aux SMPS**
  - DCM Flyback
  - QR Flyback

- **Main XFMR**
- **Optocoupler**
  - RS232

- **Sync Rect.**
  - + ORing

- **Secondary Digital Controller**

- **5Vsb/12Vsb**
- **12V**

- 90 ~ 265VAC

- ISO driver
- UART or PMBus

- **5Vsb/12Vsb**
- **12V**
Main points in the spec of a typical Server SMPS

- **Input Requirements**
  - Input Voltage Range
  - Frequency
  - Input Current Requirements
  - Harmonic Input Current Limits
  - Inrush Current
  - Efficiency
  - No Load Power Draw
  - Input Connector and Wiring

- **Output Requirements**
  - DC Load Requirements
  - Dynamic Load
  - Ripple Voltage
  - Overshoot
  - No Load Operation.
  - Common Mode Voltage and Current
  - Stability
  - Load Capacitance
Main points in the spec of a typical Server SMPS

- **Primary (Input) & Secondary (Output) Protections**
- **Power Supply Sequencing**
- **System Signals requirements**
  - Direct signals: related to the normal PSU operation
  - I²C/PMBus signals
  - Indirect Signals: Interface between the power supply and the system via registers within the power supply that are accessed by the system over the I2C bus. These registers provide the power supply status and control, ambient temperature sensors data, vital product data, power meter data, and error log data.
- **Redundancy**
  - Output Isolation OR-ing MOSFETs
  - Current Sharing Operation
  - Parallel Stability
  - Hot Swap.
- **Power Line Disturbance (PLD) Requirements**
- **EMC**
- **Environmental conditions**
- **Safety requirements**
- **Reliability**
- **Design verification/qualification and mass production guidelines**
Possible additional options

- Oversubscription: System power draw above the rating of one power supply.
- Turbo mode: Enhanced performance through processor overclocking.
- Sleep/idle states for power savings.
- AC and DC power monitoring for datacenter reporting.
- Fan speed adjustment for power/acoustics
- Calibration of DC current readback.
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HV DC/DC stage – Different topologies

**HB LLC**

- Wider range of full ZVS, even at light load. Soft switching and lower voltage peak on secondary rectification
- Higher efficiency compared to all other PWM topologies
- Critical overload protection (high stress on the device depending on controller reaction)
- Needed DSP for high power application and improving the reaction
- Hard commutation on body diode at startup, burst mode, short circuit.

**ITTF**

- High reliability: no shoot through, easy control, no requirement for MOSFET body diode.
- Higher light load efficiency than ZVS PS FB, especially in ITTF configuration
- Complete hard switching topology, therefore the efficiency is limited
- Large size compared to resonant converters (especially LLC)
HV DC/DC stage – Different topologies

- Wider range of full ZVS, even at light load. Soft switching and lower voltage peak on secondary rectification
- Higher efficiency compared to all other PWM topologies
- Lower EMI (on primary and secondary).
- Critical overload protection (high stress on the device depending on controller reaction)
- Needed DSP for high power application and improving the reaction
- Hard commutation on body diode at startup, burst mode, short circuit.

HB LLC

- Low EMI on the primary side due to soft switching
- Low switching losses due to zero voltage switching.
- Works with fixed frequency and fixed duty cycle
- Low light load efficiency.
- Critical operation conditions like short circuit, startup, burst mode (sudden reduction of duty cycle).
- Leg Short circuit issue if duty cycle of one of the switches is shorter than recovery time of the body diode of the other switch.

ITTF

03.10.2013
HV DC/DC stage – Different topologies

- **HB LLC**
  - S1
  - Cr
  - Lr
  - S2
  - S3

- **ZVS PS FB**
  - Circuit diagram showing 400VDC to 12VDC conversion with ZVS (Zero Voltage Switching) and PS (Phase Shift) feedback.
HV DC/DC Stage: choice of the topology

Figure of merit ZVS PS FB vs. HB LLC

HB LLC

- Silicon BOM opt.
- Wide Output Range
- Small Output Choke
- ZVS capability
- ZCS SR capability
- Low snubbing
- Easy thermal manage.
- High Power (Post>1KW)
- Low magnetic complex
- Efficiency
- Power density
- EMI
- Cross regulation
- No load operation
- Low Overall Cost

Phase Shift FB
LLC HB
HV DC/DC Stage: choice of the topology
Figure of merit ZVS PS FB vs. HB LLC

Phase Shift FB
LLC HB

HB LLC
## HV DC/DC Converter: Main Design Specifications

<table>
<thead>
<tr>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>350Vdc</td>
<td>380Vdc</td>
<td>410Vdc</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>11.9Vdc</td>
<td>12Vdc</td>
<td>12.1Vdc</td>
</tr>
<tr>
<td>Output Power</td>
<td></td>
<td></td>
<td>600W</td>
</tr>
<tr>
<td>Efficiency at 50%Pmax</td>
<td>97.5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>90kHz</td>
<td>150kHz</td>
<td>250Khz</td>
</tr>
<tr>
<td>Dynamic Output Voltage regulation (0-90% Load step)</td>
<td></td>
<td></td>
<td>Max overshoot =0.1V Max undershoot=0.3V</td>
</tr>
<tr>
<td>$V_{out,ripple}$</td>
<td></td>
<td></td>
<td>150mV_{pk-pk}</td>
</tr>
</tbody>
</table>
First Harmonic approximation approach

Equivalent Resonant circuit
Transfer function of the equivalent resonant circuit

\[ Mo = K(Q, m, F_x) = \left| \frac{V_{o_{ac}}(s)}{V_{in_{ac}}(s)} \right| = \frac{F_x^2(m - 1)}{\sqrt{\left( m \cdot F_x^2 - 1 \right)^2 + F_x^2 \cdot (F_x^2 - 1)^2 \cdot (m - 1)^2 \cdot Q^2}} \]

Where,

- \( Q = \frac{\sqrt{L_r/C_r}}{R_{ac}} \)
  - Quality factor

- \( R_{ac} = \frac{8}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot R_o \)
  - Reflected load resistance

- \( F_x = \frac{f_s}{f_r} \)
  - Normalized switching frequency

- \( f_r = \frac{1}{2\pi \sqrt{L_r \cdot C_r}} \)
  - Resonant frequency

- \( m = \frac{L_r + L_m}{L_r} \)
  - Ratio of total primary inductance to resonant inductance
\[ Mo = K(Q, m, Fx) \]
LLC Operation Modes

Below resonance

At resonance

Above resonance

\[ K(2, m, F) \]
\[ K(10, m, F) \]

0.1 1 10

a. \( f_0 \)
b. Below \( f_0 \)
c. Above \( f_0 \)
Design procedure: input data

\[ n = \frac{V_{in\_nom}}{2 \cdot V_{out\_nom}} \]

\[ M_{\text{min}} = K_{\text{min}}(Q, m, F_x) = \frac{n \cdot V_{o\_min}}{V_{in\_max}/2} \]

\[ M_{\text{max}} = K_{\text{max}}(Q, m, F_x) = \frac{n \cdot V_{o\_max}}{V_{in\_min}/2} \]
Design procedure
Step1: selection of $Q_{\text{max}}$
Design procedure.
Step 2: selection of $m$

Low $m$ value:
- Higher boost gain
- Narrower frequency range
- More flexible regulation

High $m$ value:
- Higher magnetizing inductance
- Lower magnetizing circulating current
- Higher efficiency
Step 3: selection of $F_{x_{\text{min}}}$

\[
\frac{d}{dF_x} K(Q, m, F_x) \bigg|_{Q_{\text{max}}} = 0.4, m = 6 = 0
\]
Design Procedure

Step 4: Voltage Gain Verification
Step 5: Calculation of resonant component values

\[ R_{ac,\text{min}} = \frac{8}{\pi^2} \cdot \frac{N_P^2}{N_S^2} \cdot \frac{V_o^2}{P_{o\text{max}}} \]

\[ Q_{\text{max}} = \frac{\sqrt{L_r/C_r}}{R_{ac,\text{min}}} \]

\[ f_r = \frac{1}{2\pi \sqrt{L_r C_r}} \]

\[ m = \frac{L_r + L_m}{L_r} \]
Summary: design flow chart

1. Select Q_max value
2. Select m value
3. Find f_xmin
4. Find k_max
   - Is k_max = required gain?
     - Yes: Solve for resonant components values
     - No: Decrease m value
   - Increase m value

END
# Prototype Specifications

## Half Bridge LLC with synchronous rectification in center tap configuration

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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</thead>
<tbody>
<tr>
<td>$V_{\text{in}}$</td>
<td>350-410V$_{\text{DC}}$</td>
</tr>
<tr>
<td>$V_{\text{in_nom}}$</td>
<td>380V$_{\text{DC}}$</td>
</tr>
<tr>
<td>$V_{\text{out_nom}}$</td>
<td>12V$_{\text{DC}}$</td>
</tr>
<tr>
<td>$I_{\text{out}}$</td>
<td>50A</td>
</tr>
<tr>
<td>$P_o$</td>
<td>600W</td>
</tr>
<tr>
<td>$f_{\text{res}}=f_0$</td>
<td>157kHz</td>
</tr>
<tr>
<td>$f_{\text{min}}$</td>
<td>90kHz</td>
</tr>
<tr>
<td>$f_{\text{max}}$</td>
<td>210kHz</td>
</tr>
</tbody>
</table>

| Transformer turns ratio    | 16:1         |
| $C_r$                      | 66nF         |
| $L_r$                      | 15.5uH       |
| $L_m$                      | 195uH        |

## Primary HV MOSFETs
- CoolMOS™ IPP60R190P6
- Reduced Gate Charge ($Q_g$)
- Reduced $E_{\text{off}}$
- High body diode ruggedness

**LLC analog controller**
ICE2HS01G
**HB Gate Drive IC**
2EDL05N06PF

## SR MOSFETs
- OptiMOS™ BSC010N04LS
- New generation
- Best FOM $R_{ds,\text{on}} \times Q_g$
- Best FOM $R_{ds,\text{on}} \times Q_{\text{oss}}$

**Bias QR Flyback controller**
ICE2QR2280Z

**Resonant inductor**
RM12 core

**Transformer**
PQ35/35 core

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PCB Boards Layout: main power board and Control and Bias daughter boards

- Power Density > 20W/inch³

Controller Board (front/back)

Bias Board
Split Capacitor technique: principle of operation

The two $C_r/2$ capacitances are dynamically in parallel and in series with $L_r$: same dynamical behaviour as typical LLC
Simulated waveforms
Bias Board Schematic
Digital Control Daughter Board Schematic

Digital Controller (DP2B/XMC)
PCB structure

PCB-Stackup

<table>
<thead>
<tr>
<th>Nr</th>
<th>Copper</th>
<th>Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.07mm</td>
<td>0.15mm</td>
</tr>
<tr>
<td>2</td>
<td>0.07mm</td>
<td>0.93mm</td>
</tr>
<tr>
<td>15</td>
<td>0.07mm</td>
<td>0.15mm</td>
</tr>
<tr>
<td>16</td>
<td>0.07mm</td>
<td></td>
</tr>
</tbody>
</table>

Gesamt: 1.51mm
Resonant tank components and related resonant frequencies

- $n = \frac{V_{in\_nom}}{2xV_o} = 380/(2*12) \approx 16$
- $L_m = 195\mu H$
- $L_r = 15.5\mu H$
- $L_n = L_m / L_r = 12.5$
- $C_r = 66nF$

\[ f_o = \frac{1}{2\pi \cdot \sqrt{L_r \cdot C_r}} = 157kHz \]

\[ f_p = \frac{1}{2\pi \cdot \sqrt{(L_r + L_m) \cdot C_r}} = 42.7kHz \]
dc-gain curve (600W LLC hardware revision E02)

\[ M_{\text{min}} = \frac{n \cdot V_{o_{\text{min}}}}{V_{\text{in}_{\text{max}}}} / 2 \]

\[ M_{\text{max}} = \frac{n \cdot V_{o_{\text{max}}}}{V_{\text{in}_{\text{min}}}} / 2 \]
Energy related calculations  
(ref. IPP60R190P6 device parameters)

\[ I_{mag\_\min} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw\_max} \cdot L_m} = 0.672 A \]

\[ En_{res\_\min} = \frac{1}{2} \cdot (L_m + L_r) \cdot I_{mag\_\min}^2 = 95.1 \mu J \]

\[ En_{cap\_\max} = \frac{1}{2} \cdot (2Co(\epsilon r)) \cdot V_{DS\_max}^2 \approx 9 \mu J \]

\[ \Rightarrow En_{res\_\min} > En_{cap\_\max} \]
Equivalent LLC circuit during dead time operation (starting at the turn-off of Q2)
$C_{HB}$ capacitances vs. half-bridge midpoint's voltage
\[ I_{Q2}(t) = I_{m, pk} \cdot (1 - \frac{t}{t_{ecs}}) \quad \forall t \leq t_{ecs} \]
\[ I_{Q2}(t) = 0 \quad \forall t \geq t_{ecs} \]

\[
 \int_{0}^{t_{dead, min}} I_{CHB}(t) \, dt = \frac{1}{2} \cdot I_{m, pk} \cdot t_{ecs} + I_{m, pk} \cdot (t_{dead, min} - t_{ecs}) = 2 \cdot Q_{oss}, @ 400V
\]

\[ t_{dead, min} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss}, @ 400V}{I_{m, pk}} \]
Time related calculations
(ref. IPP60R190P6 device parameters)

\[ I_{m ag \_ min} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw \_ max} \cdot L_m} = 0.672 A \]

\[ I_{m ag \_ max} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_o}{2\pi \cdot f_{sw \_ min} \cdot L_m} = 1.66 A \]

\[ t_{dead, \ min} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss, @ 400V}}{I_{m ag, \ max}} \approx 130 n \text{sec} \]

\[ t_{dead, \ max} = \frac{t_{ecs}}{2} + \frac{2 \cdot Q_{oss, @ 400V}}{I_{m ag, \ min}} \approx 311 n \text{sec} \]
Main transformer structure: PQ35/35 core with TDK PC95 ferrite material

### LLC main transformer

<table>
<thead>
<tr>
<th>Core form and material</th>
<th>PQ35/35, PC95 (TDK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bobbin</td>
<td>Epcore, B6882E0012Y001</td>
</tr>
<tr>
<td>Primary inductance $L_p$</td>
<td>195uH, measured between 2.3 and 4.5, other pins open</td>
</tr>
<tr>
<td>Leakage inductance $L_a$</td>
<td>1.5uH, measured between 2.3 and 4.5, other pins shorted</td>
</tr>
<tr>
<td>Isolation voltage $V_{iso}$</td>
<td>2500Vrms / 50Hz, 1min (between 2,3,4,5 and A,B,C)</td>
</tr>
</tbody>
</table>

**Core Center Limb**

- **Pin 1, 2, 3, 4, 5, 6:** Winding arrangements
  - Pin 4.5: Winding 4: 8 turns/ 2 times 90x0.1 Litz / 1 layer / tight
  - Pin 2.3: Winding 1: 8 turns/ 2 times 90x0.1 Litz / 1 layer / tight
  - Winding 3: 1 turn / copper foil 0.5mm*20mm
  - Winding 2: 1 turn / copper foil 0.5mm*20mm

**Connection of secondary copper foil:**

### Technical Data Sheet

- **Core / material / air gap:** PQ35/35 / K2008 or equiv. / 0.25
- **Nominal inductance:** $L1+LV1 = 195\mu\text{H} \pm 15\%$
- **Ratio of transformation:** 8 : 1 : 8
- **Dielectric strength (50Hz/1s):** 2.5kV (prim - sec)
- **Leakage inductance:** max. 3\muH
- **Operating temperature:** -25°C - +125°C
- **Storage temperature:** -25°C - +85°C
- **Humidity / application class:** F (DIN 40040)
Resonant choke: RM12 core, material N87

<table>
<thead>
<tr>
<th>Core form and material</th>
<th>RM12, N87 (Epcos)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bobbin</td>
<td>Epcos, B65816C1512T001</td>
</tr>
<tr>
<td>Inductance L</td>
<td>14uH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Windings</th>
<th>Start</th>
<th>End</th>
<th>Wire</th>
<th>Turns</th>
<th>Layers</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>N1</td>
<td>7,8,9</td>
<td>10,11</td>
<td>120x0.1mm Litz</td>
<td>9</td>
<td>1</td>
<td>Tight</td>
</tr>
</tbody>
</table>

Technical Data Sheet

Customer: Infineon Technologies
Part designation: SP-RM 12
Customer part number:

<table>
<thead>
<tr>
<th>Core / material / air gap</th>
<th>RM12 / K2008 or equiv., 1,1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal inductance</td>
<td>L = 14μH ± 15%</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-25°C ~ +125°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>-25°C ~ +85°C</td>
</tr>
<tr>
<td>Humidity-/application class</td>
<td>F (DIN 40040)</td>
</tr>
</tbody>
</table>
Efficiency plot at $V_{in}=380\,V_{dc}$
10%Pmax Vin=380Vdc

Loossses spread on each device at 10%Pmax [W]

- Turn-off losses
- Body diode losses
- Driving losses
- Conduction Losses

10%Pmax Overall losses spread [W]

- Tracks, Cin, sensing
- Output capacitance
- Output choke
- Resonant choke
- SR losses
- Power trafo
- Primary mosfets (IPP60R190P6)

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50%Pmax Vin=380Vdc

Losses spread on each device at 50%Pmax [W]
- Turn-off losses
- Body diode losses
- Driving losses
- Conduction Losses

50%Pmax Overall losses spread [W]
- Tracks, Cin, sensing
- Output capacitance
- Output choke
- Resonant choke
- SR losses
- Power trafo
- Primary mosfets (IPP60R190P6)
100%P\text{max} \text{ Vin}=380\text{Vdc}

- Turn-off losses
- Body diode losses
- Driving losses
- Conduction losses

Loosses spread on each device at 100%P\text{max} \text{ [W]}

100P\text{max} Overall losses spread \text{ [W]}

- Tracks, Cin, sensing
- Output capacitance
- Output choke
- Resonant choke
- SR losses
- Power trafo
- Primary mofets (IPP60R190P6)
Summary of the digital control expected additional features compared to ICE2HS01G

<table>
<thead>
<tr>
<th>Feature</th>
<th>Concept</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adaptive dead time primary MOSFETs (during operation)</td>
<td>Dead time variable in function of $I_{\text{load}}$ and $V_{\text{in}}$</td>
</tr>
<tr>
<td>Prevention of hard commutation (e.g. at start-up)</td>
<td>Mixed mode between PFM and PWM</td>
</tr>
<tr>
<td>Prevention of capacitive mode operation</td>
<td>Voltage reading on low side MOSFET sense resistor</td>
</tr>
<tr>
<td>Improve transient response compared to analog control (&lt;20usec)</td>
<td>Faster change in switching frequency (e.g. during dynamic load) compared to analog control</td>
</tr>
<tr>
<td>Fully digital control loop</td>
<td>Zero and poles of the transfer function digitally predetermined (only applicable if the controller is on secondary side)</td>
</tr>
<tr>
<td>Automatic loop compensation in function of different $C_{\text{out}}$</td>
<td>Create various sets of selectable zeros and poles (only applicable if the controller is on secondary side)</td>
</tr>
<tr>
<td>Independently change duty cycle on primary and secondary MOSFETs</td>
<td>TBD</td>
</tr>
<tr>
<td>Fast change of PWM frequency without losing synchronization between PWM channels</td>
<td>TBD</td>
</tr>
<tr>
<td>Fast ADC converter for OCP</td>
<td>TBD</td>
</tr>
</tbody>
</table>

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